Radu M. Secareanu

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Education

- Ph.D.E.E. – April 2000, University of Rochester, Rochester, NY
    - Dissertation title: "On the Interdependence of Substrate Coupling on Technology, Circuit, and Physical Design in Mixed-Signal Smart-Power Circuits"
- M.S.E.E. – June 1990, Polytechnic University of Bucharest, Romania

Experience

- 2021-present – RecResearch Semiconductors (RecResearch-Semi.com) – Founder
    - Highlights:
        - Developed enablers for "Next Generation Digital Communication, Data Storage, and Data Security". A patent portfolio is being developed, with five patents currently filed and more in development. Software emulators are being developed. The target is to develop specialized chips in partnership with established companies, chips that implement this IP.
- 2000-2021 – Motorola Inc. -> Freescale -> NXP --- Senior Principal R&D Engineer, Phoenix, AZ
    - Highlights:
        - Lead: Defining design strategies, implementations, floor plans, integration (chip-level and chip/package/pcb) and conducting simulation, characterization, analysis, qualification, CQI, in term of signal isolation/interference for products and design teams across the company
            - Products:
                - RF: Car-to-Car communication, Automotive Radar, Car Radio, Cellphone, Zigbee, Bluetooth, Medical, etc.
                - Buck-converter/CAN/LIN integration
                - Microcontrollers
        - Product modeling, support, verification, qualification and debug for EMC/on-chip emissions compliance, EFT, latch-up and parasitic BJT
        - Develop, evaluate, qualify infrastructure for modeling and simulation applicable to aforementioned activities and products, from technology/TCAD/PDK, to design rules and best practices, to methodology, design flows, and tools
        - Develop methodologies and niche internal tools
            - For signal isolation/interference
                - Placement and sizing of on-chip decoupling capacitors, power grid design, and power delivery
                - Integrated Circuit Emissions Modeling (ICEM)
                - Chip-package-pcb co-design
            - For prediction and prevention of small and large signal parasitic bipolar effects

        - Locate, characterize, model, and report risky parasitic bipolars (NPNs, PNPs, SCRs) in a GDS design database
    - Circuit design using reconfigurable and adaptive architectures (analog, low-voltage, high noise immunity)
  - Latch-up and parasitic bipolar predictive analysis and verification of products across company, as well as post-failure debug analysis
  - Provide training and guidance for design teams in signal integrity and latch-up fundamentals and techniques for design, prevention, and optimizations
  - Research coordinator of six summer internships
- 2002-present – Arizona State University (ASU) --- EEE Adjunct Professor, Tempe, AZ
  - Taught more than 25 class sessions (more than 1,000 students) – mostly graduate level (such as Digital VLSI Design) and some undergraduate level (Analog Design)
- 1996-2000 – Xerox Corporation and Kodak Corporation – Rochester N.Y.
  - Year-round intern funding my Ph.D., working on design, test, and evaluation of noise isolation and signal integrity aspects for inkjet printer circuits and imaging sensors/circuits
- 1990-1995 – Baneasa S.A. Semiconductors --- Analog design engineer, Bucharest, Romania
  - Analog circuit design for consumer products, primarily bipolar, including op-amps, audio amplifiers, ADC/DAC converters. Prototype sample characterization and qualification, product data sheet and product standard development, customer design reviews
- 1994-1995 – Research Institute for Electronic Components (ICCE) – Associate R&D Engineer, Bucharest, Romania

___Publications, Patents, External Research, Memberships, Awards, Recognitions___

- Author and co-author of more than 50 journal and conference papers
- Inventor and co-inventor of more than 20 issued and pending patents, US and international
- Inventor of five pending patents, owning all rights
- Author and co-author of several defensive publications
- Research coordinator of six summer internships at Motorola/Freescale
- IEEE Member
- TPC Member, Session chair, Track chair, Publications chair for various IEEE Conferences
- Associate Editor and Guest Editor for various IEEE Journals, Reviewer for IEEE Journals and Conferences
- Recognized by Freescale CEO (Gregg Lowe) and CTO (Ken Hansen) for my work in the development of methodology/tool for latch-up and parasitic bipolar prediction and prevention
- Recipient of multiple awards, among which the *"SRC/GRC Mahboob Khan Outstanding Mentor Award", "SRC/GRC Mentor Award", "Freescale Outstanding Liaison Award", "Freescale RF Division Training Award"*
- Various tutorials, such as at EMCcompo, RFIC, ISCAS, SOCRT, IEEE Phoenix Section
- Outstanding SRC/GRC activities including University associations for SRC/GRC research projects